Patent Claims

1. Method for feature modification given one-dimensional signals converted into a digital representation upon employment of the adaptive overlap-add algorithm, which implements the feature modification after a suitable, discrete spectral transformation by multiplication in the frequency domain and subsequently generates the output signal by corresponding, inverse, discrete spectral transformation as well as by overlapping and shifted addition of a plurality of signal segments supplied by the inverse spectral transformation, characterized in that, before the multiplication in the frequency domain, the frequency response function is convoluted with a selectable, discrete window function that exhibits a considerably shorter length than the frequency response function.

2. Method according to claim 1, characterized in that the window function comprises only positive values and a smooth curve in the frequency domain but comprises a pronounced structure in the time domain with a large, positive principal lobe and secondary maximums and secondary minimums that are small in terms of amount.

3. Method according to claim 1, characterized in that the spectral transformation can be fashioned as discrete Fourier transformation and the inverse spectral transformation can be fashioned as inverse discrete Fourier transformation.

4. Method according to claim 3, characterized in that the discrete Fourier transformation and the inverse discrete Fourier transformation are implemented with the assistance of the algorithm of fast Fourier transform (FFT).

5. Method according to claim 1, characterized in that the spectral transformation is fashioned as discrete cosine transformation (cosine transform) and the inverse spectral transformation is fashioned as inverse discrete cosine transformation.

6. Method according to claim 1, characterized in that the spectral transformation is fashioned as discrete Haar transformation and the inverse spectral transformation is fashioned as inverse Haar transformation.

7. Method according to claim 1, characterized in that the spectral transformation is fashioned as discrete Walsh-Hadamard transformation and tyhe inverse spectral transformation is fashioned as inverse Walsh-Hadamard transformation.

8. Method according to claim 1, characterized in that the spectral transformation is fashioned as discrete Hartley transformation and the inverse spectral transformation is fashioned as inverse Hartley transformation.

9. Method according to claim 2, characterized in that the window with which the frequency response function is convoluted is acquired by discretization from known, continuous window functions, whereby the curve originally provided for the time domain can be applied in the frequency domain.

10. Method according to claim 9, characterized in that the window with which the frequency response function is convoluted is calculated and stored before the beginning of the processing.

11. Method according to claim 9, characterized in that the window with which the frequency response function is convoluted is recalculated given every processing of a block of n spectral values.

12. Method according to claim 2, characterized in that the window with which the frequency response function is convoluted represents the discretization of a prolate spheroidal window function, whereby the curve originally provided for the time domain can be applied in the frequency domain.

13. Method according to claim 2, characterized in that the window with which the frequency response function is convoluted can be modified during the processing dependent on an error information acquired from the output signal.

14. Device for the implementation of the method according to one or more of the claims 1 through 13, characterized in that the shift registers 40, 130, 131, 134, 180 and 190, the multipliers 70, 120 and 133, the adders 136 and 170, the memories 80 and 137, the transformation unit 100, the inverse transformation unit 160 and the switch 200 are fashioned as digital circuits.

15. Device according to claim 14, characterized in that the digital circuits are constructed of standardized digital circuits.

16. Device according to claim 14, characterized in that the digital circuits, a control unit as well as the connecting lines between these can be realized on a semiconductor chip with doping, etching and metal deposition process steps of microstructure technology.

17. Device for the implementation of the method according to one or more of the claims 1 through 13, characterized in that the method is represented as a sequence of microprogram words that can be applied in a microprogram control unit.

18. Device for the implementation of the method according to one or more of the claims 1 through 13, characterized in that the method is represented as a sequence of assembler commands that can be implemented on a microcomputer or on a specialized signal processor.

19. Device according to claim 18, characterized in that the sequence of assembler commands is generated by a compiler program that takes the information required therefor from a program written in a higher programming language.